Chapter 4

BLOCK DIAGRAMS FOR CONTROL LOGIC

This chapter describes the main block diagrams for the control logic of the FRENIC-Mini series of inverters.

Contents

FRENIC-Mini inverters are equipped with a number of function codes to match a variety of motor operations required in your system. Refer to Chapter 9 "FUNCTION CODES" for details of the function codes.

The function codes have functional relationship with each other. Several special function codes also work with execution priority with each other depending upon their data settings.

This chapter contains the main block diagrams for control logic in the inverter and describes the relationship between the inverter's logic and function codes. It is important to fully understand this relationship and to set the function code data correctly.

The block diagrams contained in the chapter show only function codes having mutual relation. For the function codes that work stand-alone and for details of individual function codes, refer to Chapter 9 "FUNCTION CODES."

4.1 Symbols Used in the Block Diagrams and their Meanings

Table 4.1 lists the symbols commonly used in the block diagrams and their meanings with some examples.

Table 4.1 Symbols and Meanings

Symbol	Meaning
[FWD],[Y1] (etc.)	Input/output signals to/from the inverter's control terminal block.
(FWD),(REV) (etc.)	Control commands assigned to the control terminal block input signals.
Set Frequency	Internal control command for inverter logic.
F15	High limiter: Limits peak value by a constant or by data set to the function code.
F16	Low limiter: Limits the bottom value by a constant or by data set to the function code.
"0"	Zero limiter: Keeps data from dropping to a negative value.
A, B, X, C	Gain multiplier for set frequencies given by current and/or voltage input or for analog output signals. C = A × B
A, B, +, +, C	Adder for 2 signals or values. C = A + B If B is negative then C = A – B.

Symbol	Meaning
F01	Function code.
E01, 7, 8, 19	Switch controlled by a function code. Numbers assigned to the terminals express the function code data.
Link Command (LE)	Switch controlled by an internal control command. In the example shown at the left, the link operation command (LE) is assigned to one of the digital input terminals from [X1] to [X3], which then controls the switch.
	Low-pass filter: Features appropriate characteristics by changing the time constant through the function code data.
A, B, C	AND logic: In normal logic systems, only if A = ON and B = ON, then C = ON. Otherwise, C = OFF.
A, B, C	OR logic: In normal logic systems, if any inputs are ON, then C = ON. Only if all inputs are OFF, then C = OFF.
A, B	NOT logic: In normal logic systems, if A = ON, then B = OFF and vice versa.

4.2 Drive Frequency Command Generator

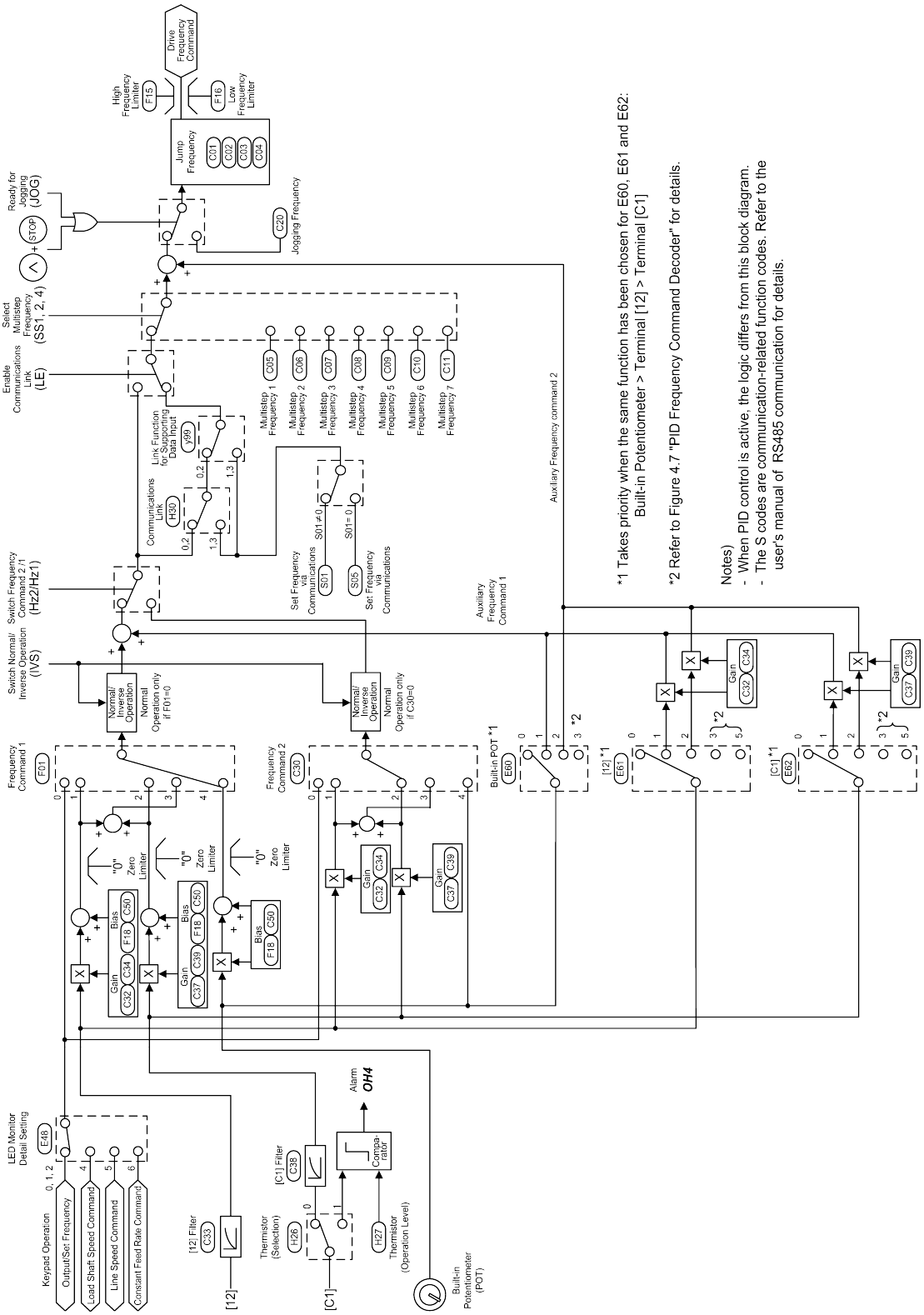

Figure 4.1 Block Diagram for Drive Frequency Command Generator

Figure 4.1 shows the processes that generate the final drive frequency command from the frequency settings given by various means and those switched/modified by function codes. If PID process control takes effect (J01=1 or 2), the drive frequency generation will differ from that shown in this diagram. (Refer to Section 4.8 "PID Frequency Command Generator.")

Additional and supplemental information is given below.

- Frequency settings using the ⌃ / ⌄ key on the keypad may take a different format by means of the data setting for function code E48. Refer to function code E48 in Chapter 9 "FUNCTION CODES" for details.
- [C1] input as a frequency settings signal will always be interpreted as "0" when the current input signal terminal [C1] is specified for the thermistor (H26 = 1).
- Settings for both gain and bias will take effect concurrently only for frequency setting 1 (F01). For frequency setting 2 (C30) and auxiliary frequency settings 1 and 2 (E60 to E62), only the gain will take effect.
- Gain for the built-in potentiometer cannot be changed by any function code or other means.
- Switching between normal and inverse operation is only effective for frequency setting from the analog input signal (terminal [12], [C1] or built-in potentiometer). Frequency settings from the ⌃ / ⌄ key are only valid for normal operation.
- The command formats for frequency settings by S01 and S05 for the communications link facility take a different form, as follows:
    - S01: the setting range is –32768 to +32767, where the maximum output frequency is obtained at ±20000.
    - S05: the setting range is 0.00 to 655.35 Hz in 0.01 Hz step, or 0.1 Hz step for over 600 Hz.
    - Priority level for setting for S01 is higher than that for S05. If a value other than 0 is set for S01, then the data set to S01 will take effect. If S01 = 0, then the setting for S05 will take effect.
    - Refer to the RS485 Communication User's Manual (MEH448) for details.

4.3 Drive Command Generator

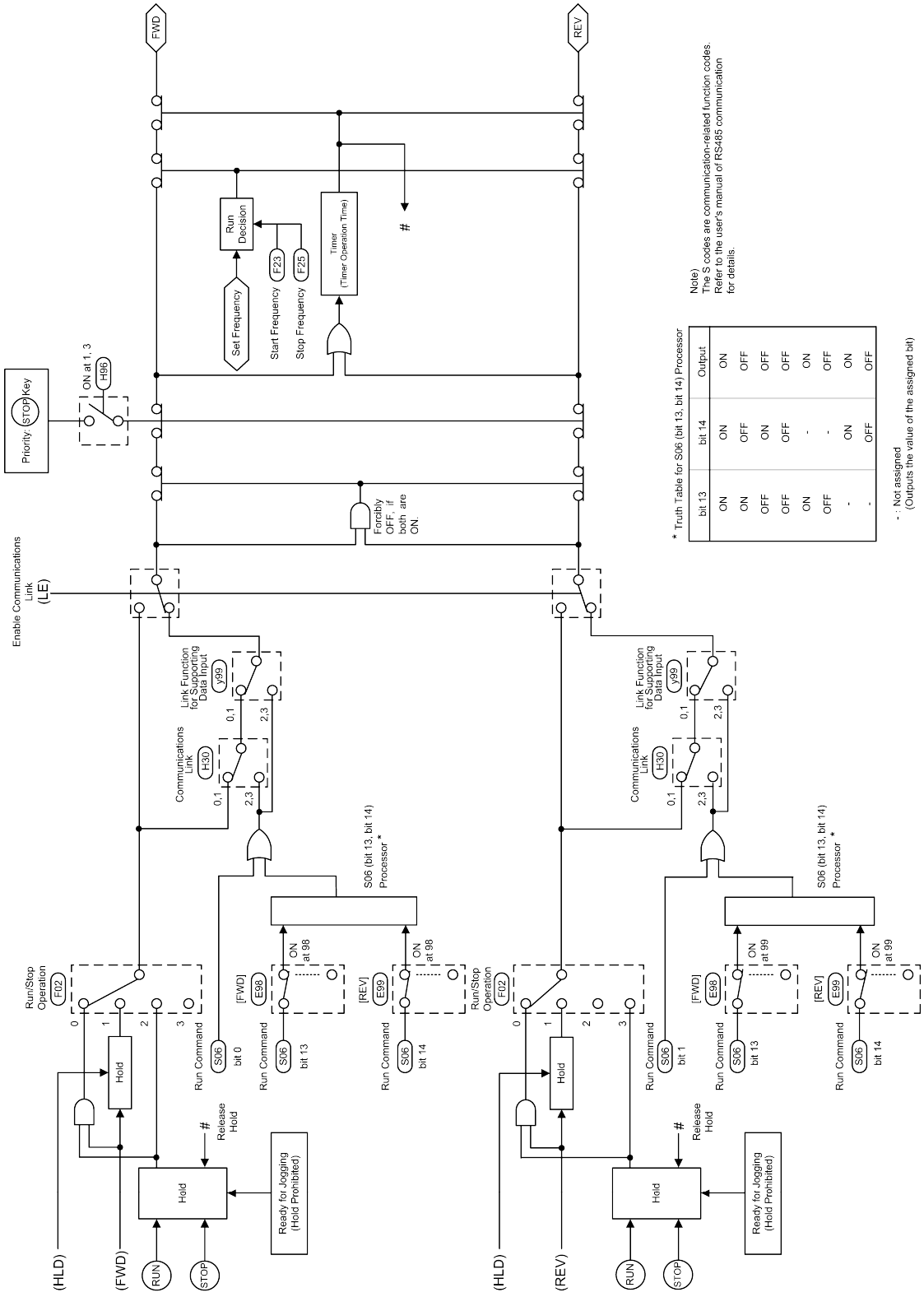

Figure 4.2 Drive Command Generator

The drive command generator shown in Figure 4.2 produces final drive commands (FWD: Drive the motor in the forward direction) and (REV: Drive the motor in reverse direction) from the run commands that are given by various means and modified/switched by function codes.

Additional and supplemental information is given below.

- For the run command given by the (RUN) / (STOP) key, the generator holds the command ON upon depression of the (RUN) key and releases it upon depression of the (STOP) key except during jogging operation.
- The hold command (HLD) holds the run forward/reverse commands (FWD)/(REV) until it is turned OFF. This allows you to run the inverter in "3-Wire Operation." Refer to the function code E01 in Chapter 9 "FUNCTION CODES" for details.

  If you do not assign a hold command (HLD) to any digital input terminals, then the "2-Wire Operation" using the (FWD) and (REV) command will be active.
- Setting 0 (zero) for function code F02 allows you to operate the inverter using the (RUN) / (STOP) key on the built-in keypad for the run command, while the (FWD) and (REV) commands determine direction of motor rotation. The logic shown in the block diagram shows you that if the run command from the (RUN) key and either the (FWD) or (REV) command are given, then the internal run command <FWD> or <REV> decoded internally by the logic turns ON.
- S06 (2-byte data for bit 15 through bit 0 can be manipulated), the operation command by the communications link, includes:
  - Bit 0: assigned to (FWD)
  - Bit 1: assigned to (REV)
  - Bits 13 and 14: programmable bits equivalent to the terminal inputs [FWD] and [REV]
  - In the block diagram, all of these are noted as operation commands. The data setting for function code E98 to specify the terminal signal property for [FWD] and E99 for [REV] determine which bit value should be selected as the run command. If bits 13 and 14 have the same setting to specify the property for (FWD) or (REV), the output of bit 13-14 processor logic will follow the truth table listed in Figure 4.2.
  - If either one of bits 13 and 14 is ON (1 as logic value), the OR logic will make the link command (LE) turn ON.
- If both run commands (FWD) and (REV) come ON concurrently, the logic forces the internal run commands <FWD> and <REV> to immediately turn OFF.
- If you set 1 or 3 to function code H96 (STOP key priority/Start Check) to make the (STOP) key priority effective, then depressing the (STOP) key forces the internal run commands <FWD> and <REV> to immediately turn OFF.
- If you have enabled operation via the timer, inputting any run command starts the timer. The internal run command <FWD> or <REV> and hold command (HLD) triggered by keypad will be automatically turned OFF after the time preset in the timer has elapsed.
- If the set frequency is lower than the start frequency (F23) or the stop frequency (F25), the internal run commands will remain OFF.

4.4 Terminal Command Decoders

Figures 4.3 (a) through (d) show five types of the terminal command decoder for the digital input signals.

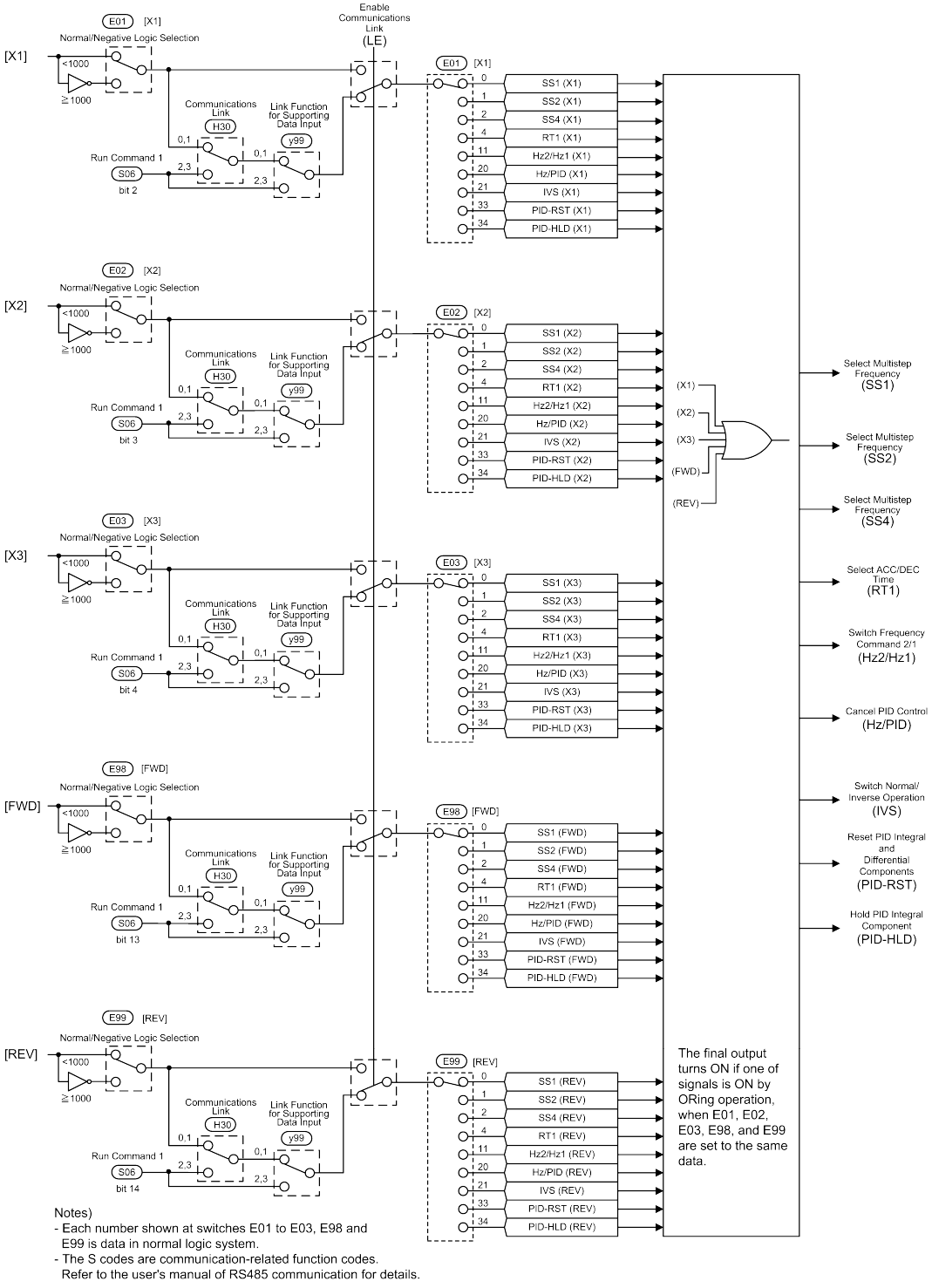

Figure 4.3 (a) Terminal Command Decoder (General)

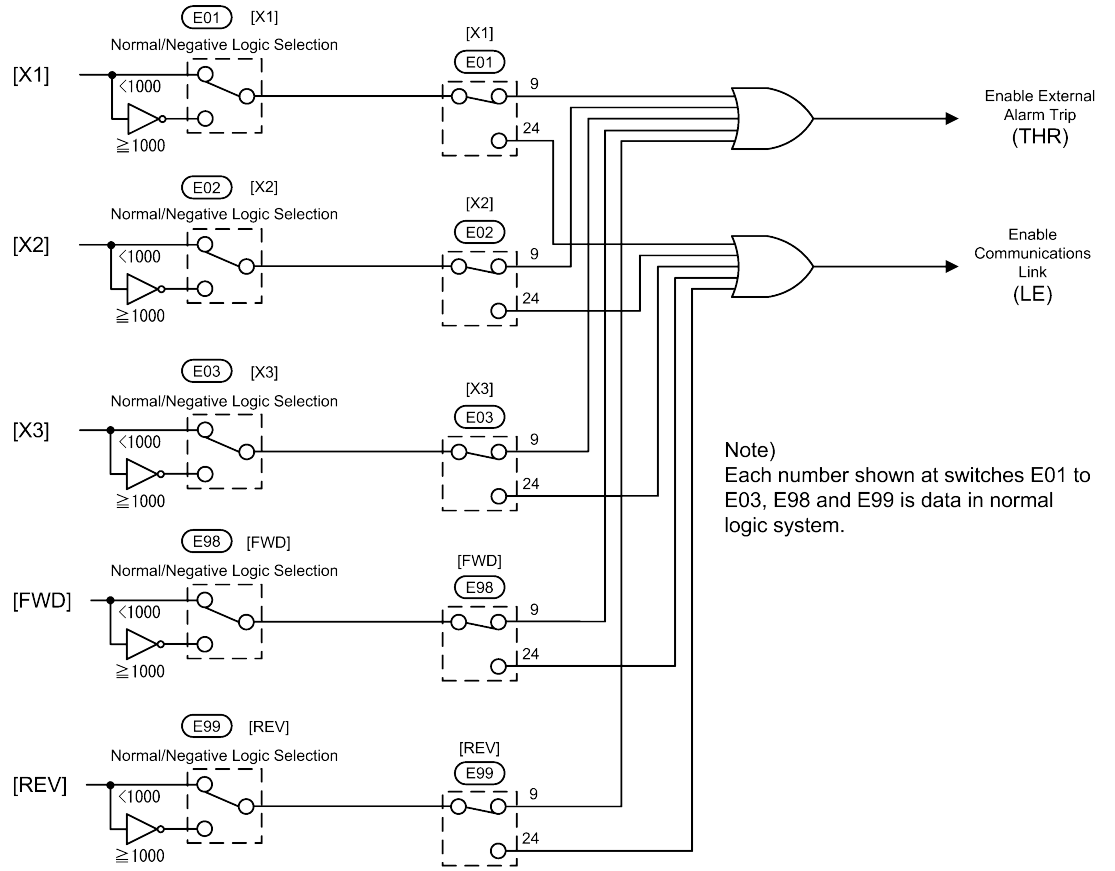

Figure 4.3 (b) Terminal Command Decoder (Terminal Signal Inputs)

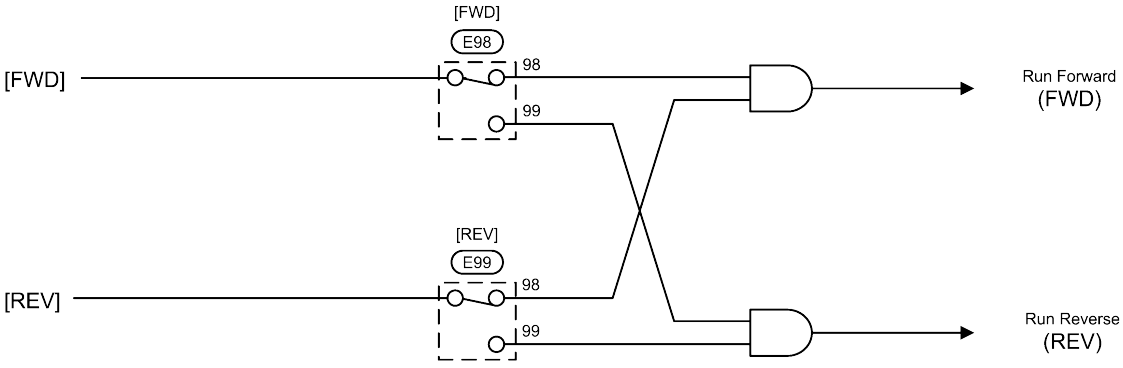

Figure 4.3 (c) Terminal Command Decoder (Terminal Signal Input Excluding Negative Logic)

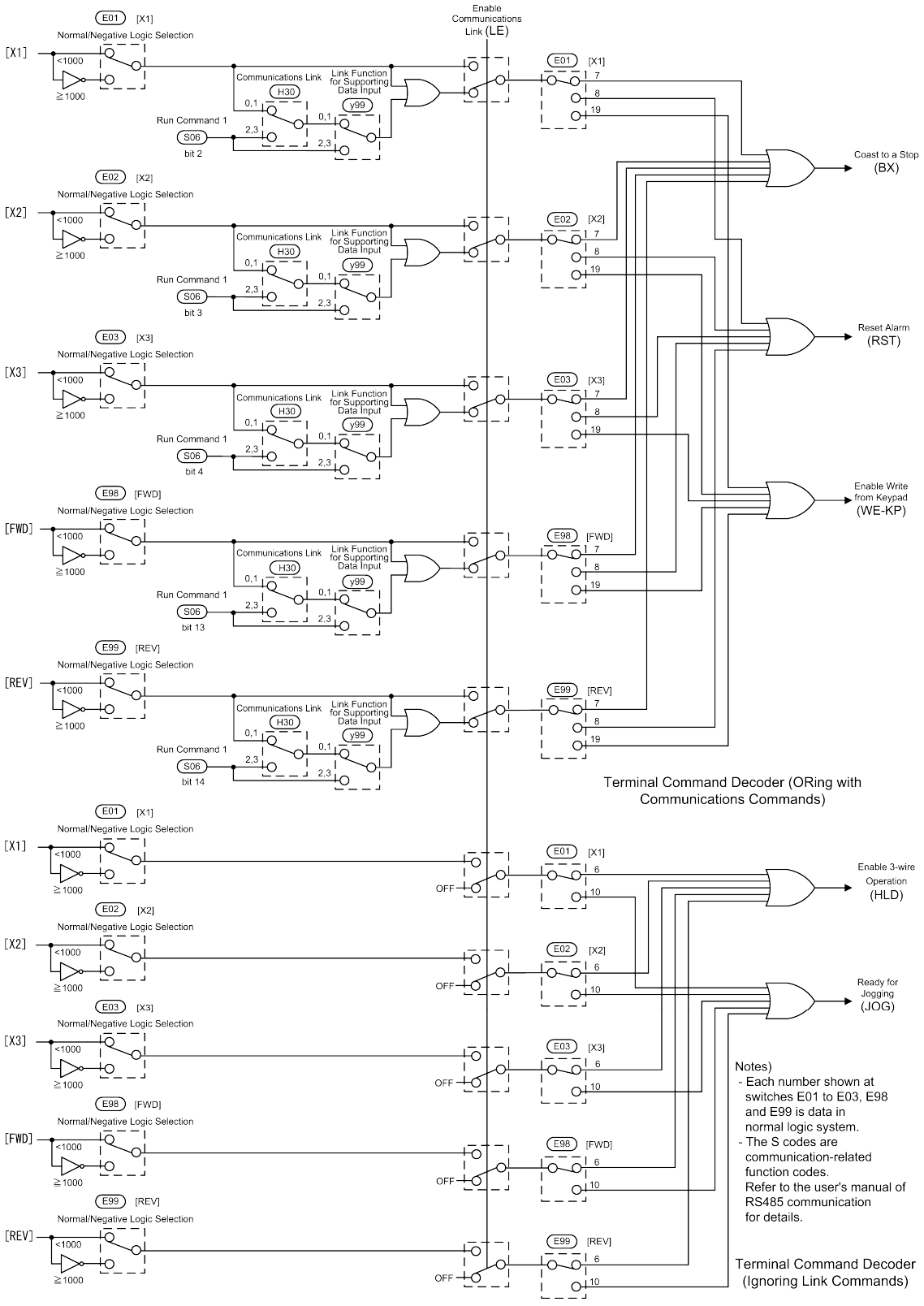

Figure 4.3 (d) Terminal Command Decoder (ORing with Link Commands/Ignoring Link Commands)

Programmable digital input terminals [X1], [X2], [X3], [FWD] and [REV] can be assigned to internal terminal commands such as (FWD) or (REV) decoded by data settings of related function codes as shown in the block diagrams in Figures 4.3 (a) through 4.3 (d). In the decoders, negative logic input signals are also applicable if you set data of 1000s to the function code.

The contents of the block diagram are divided into five groups, depending on whether inputs are assigned for the same internal terminal commands respectively or the commands issued from the communications facility (linked operation) specify the internal commands. Each of the diagrams shown in Figure 4.3 has following role.

- Figure 4.3 (a) The terminal command decoder (general) shows the decoding process of the internal commands functioning with the negative logic inputs. This is switchable with inputs from the communications facility (for example, link operation commands received through RS485 communications).
- Figure 4.3 (b) The terminal command decoder (terminal signal inputs) shows the process to decode internal terminal commands dedicated to the control signal input applied to the inverter's terminal block. These commands cannot be changed via the communications facility (link operation command).
- Figure 4.3 (c) The terminal command decoder (terminal signal input excluding negative logic) shows process to produce (FWD) and (REV) commands. In this process, settings via the communications facility do not take effect. In the next process of the drive command generator, however, they may take effect. (Refer to the block diagram in Section 4.3, "Drive Command Generator.") To keep the inverter operation safe, any negative logic input for the (FWD) and (REV) commands cannot be applied.
- Figure 4.3 (d) The upper part of the terminal command decoder (ORing with link commands/ignoring link commands) shows the process to produce commands by ORing signals issued from the communications facility and the control signal input terminal block (Logical Oring. If any of input signals is ON, then the command becomes ON.).
- Figure 4.3 (d) The lower part of the terminal command decoder (ORing with link commands/ignoring link commands) shows the process to produce commands by forcing the inverter to ignore signals issued from the communications facility even if link operation ((LE): link operation command) has been turned ON.

4.5 Digital Output Selector

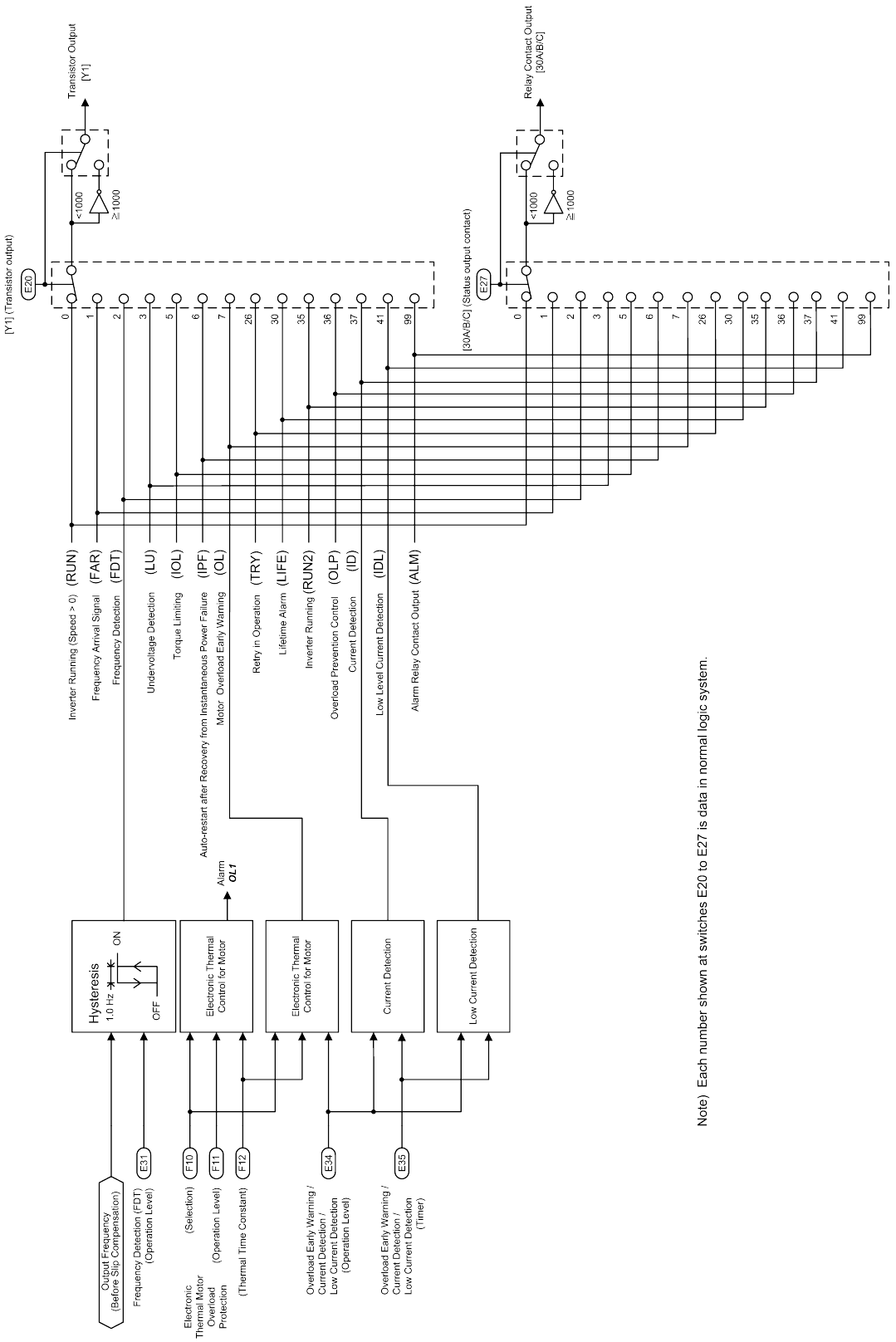

Figure 4.4 Digital Output Signal Selector

The block diagram shown in Figure 4.4 shows you the processes to select the internal logic signals for feeding to two digital output signals [Y1] and [30A/B/C]. The output terminals [Y1] (a transistor switch) and [30A/B/C] (mechanical relay contacts) are programmable. You can assign various functions to these terminals using function codes E20 and E27. Setting data of 1000s allows you to use these terminals for the negative logic system.

4.6 Analog Output (FMA) Selector

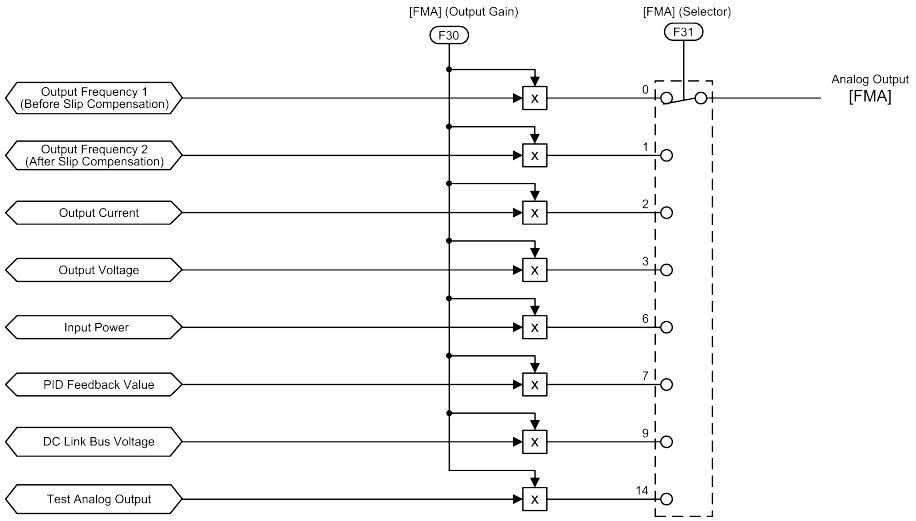

Figure 4.5 Analog Output (FMA) Selector

The block diagram shown in Figure 4.5 shows the process for selecting and processing the analog signals to be outputted to the analog output terminal [FMA]. Function code F31 determines the signals to be outputted to [FMA]. Function code F30 scales the output signal to a level suitable for the meters to be connected to the [FMA] terminal.

The output voltage range is 0 to 10 VDC and the maximum allowable load current is 2 mA. This is capable of driving two analog voltmeters with a common rating.

The test analog output is full-scale voltage output that adjusts the scale of the connected meter.

4.7 Drive Command Controller

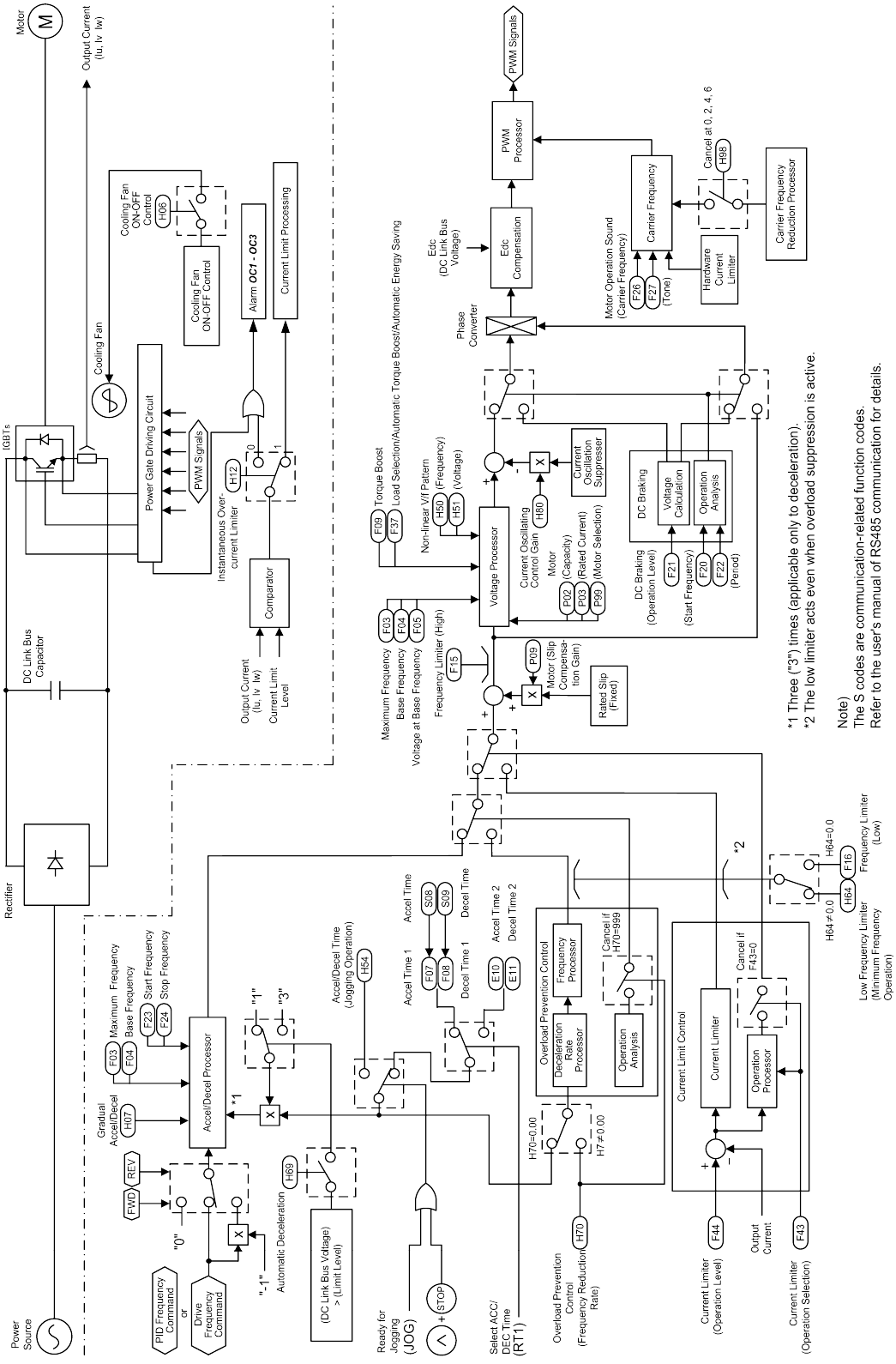

Figure 4.6 Drive Command Controller and Related Part of the Inverter

The simplified block diagram shown in Figure 4.6 explains the process in which the inverter drives the motor according to the internal run command <FWD>/<REV> from the frequency generator, or the PID frequency command from the PID controller, and the run commands.

Additional and supplemental information is given below.

- The logic shown in the left part of the block diagram processes the drive frequency command so as to invert (×(-1)) the command for reverse rotation of the motor or to replace it with 0 (zero) for stopping the motor.
- The accelerator/decelerator processor determines the output frequency of the inverter by referring to the set data of related function codes. If the output frequency exceeds the peak frequency given by function code F15, the controller limits the output frequency at the peak.
- Acceleration/deceleration time is selectable from acceleration/deceleration time 1 or 2, or acceleration/deceleration time for jogging operation. The suppression of the regenerative braking feature may multiply the commanded acceleration/deceleration time by 3. Refer to role of function code H69 in the block diagram.
- If the overload prevention control feature is active, then the logic automatically switches the output frequency to one of overload suppression control and controls the inverter using the switched frequency.
  However, if the current limit control is active (F43 ≠ 30, H12 = 1), the overload prevention control automatically becomes inactive.
- If the current limit control is active, then the logic automatically switches the output frequency to one of current limit control and controls inverter using the switched frequency.
- The slip compensation facility adds frequency components calculated from the load based on the preset rated slip frequency inside the inverter to the frequency currently commanded. The logic adjusts the error between the rated slip frequency of the motor currently under load and the preset frequency according to the set data of function code P09 that controls slip compensation gain for the motor.
- The voltage processor determines the output voltage of the inverter. The processor adjusts the output voltage to control the motor output torque.
- If DC braking control is active, the logic switches the voltage and frequency control components to ones determined by the DC braking block to feed the proper power to the motor for DC braking.

4.8 PID Frequency Command Generator

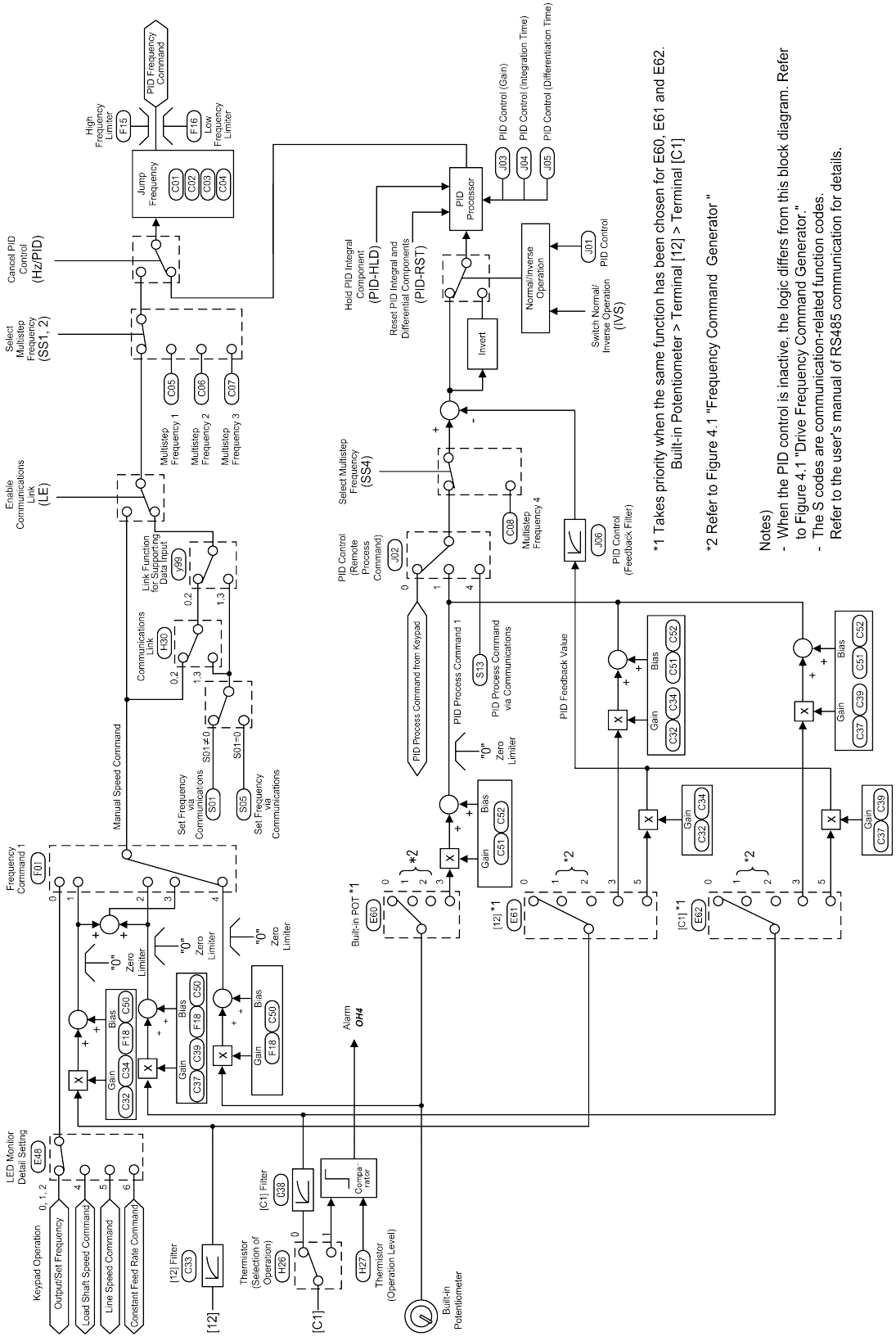

Figure 4.7 PID Frequency Command Generator

The block diagram shown in Figure 4.7 shows the PID frequency command generator that becomes active when the PID control is enabled (J01= 1 or 2). The logic shown generates the final frequency command according to the PID process command given by various means of setting and feedback, or frequency settings as a speed command given manually, and various means of switching.

Additional and supplemental information is given below.

- Switching of data settings for frequency 2 (C30), auxiliary frequencies 1 and 2 (E60 to E62) as manual speed commands will be disabled.
- For multistep frequency settings, settings 1 to 3 are exclusively applicable to the manual PID speed command.
- For selecting analog input (terminal [12], [C1], or built-in POT) as the PID process command, you need to set proper data for function codes E60 to E62 and J02.
- For the multistep frequency, setting data 4 (C08) is exclusively applicable to PID process command.
- To switch the operation between normal and inverse, the logic inverses polarity of deviation between the PID command and its feedback (turning (INV) command ON/OFF, or setting J01 = 1 or 2).
- Refer to Section 4.2 " Drive Frequency Command Generator" for explanations of common items.